

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization  
International Bureau



(43) International Publication Date  
18 December 2003 (18.12.2003)

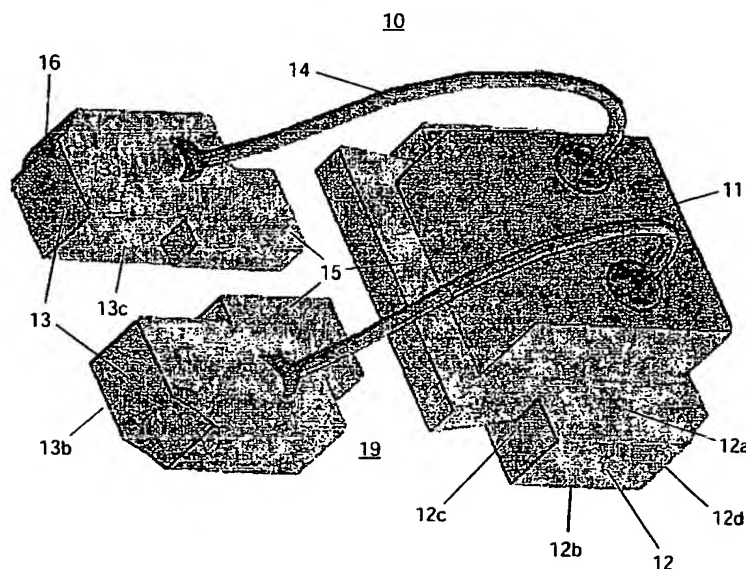
PCT

(10) International Publication Number  
**WO 03/105223 A2**

- (51) International Patent Classification<sup>7</sup>: **H01L 23/31, 23/495**
- (21) International Application Number: **PCT/IB03/02094**
- (22) International Filing Date: **4 June 2003 (04.06.2003)**
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data:  
02012603.3 **6 June 2002 (06.06.2002) EP**
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- (81) Designated States (national): **AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.**
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- (84) Designated States (regional): **ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,**

[Continued on next page]

(54) Title: **QUAD FLAT NON-LEADED PACKAGE COMPRISING A SEMICONDUCTOR DEVICE**



(57) Abstract: A semiconductor package is proposed. The semiconductor package includes a discrete semiconductor chip on a die pad; a plurality of bond pads situated next to the chip and formed with a plurality of connecting mechanisms and an encapsulant for encapsulating the chip and the pads. In a preferred embodiment the die pad and/or the bond pads comprise means for vertically and laterally interlocking the pads to the encapsulant. The interlocking means of the bond pads and the die pad significantly enhance the bonding strength between the pads and the encapsulant for preventing delamination or cracking, so that quality and reliability of the quad flat non-leaded semiconductor package comprising a discrete can be assured.

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ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,  
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,  
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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**Published:**

— *without international search report and to be republished  
upon receipt of that report*

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23/495

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PCT/TB2003/002094

(22) International Filing Date: 4 June 2003 (04.06.2003)

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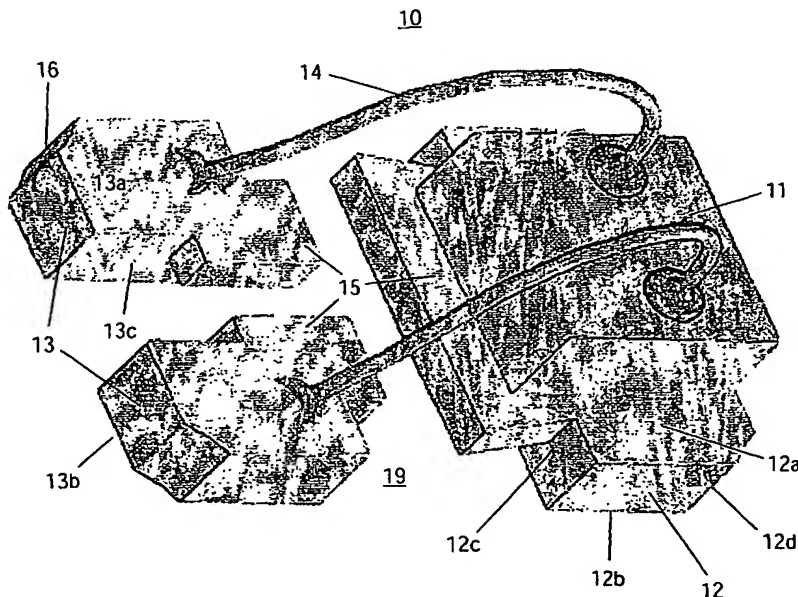
(74) Agent: **VOLMER, Georg;** Philips Intellectual Property &  
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CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,  
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,  
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MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD,  
SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US,  
UZ, VC, VN, YU, ZA, ZM, ZW.

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European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,  
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WO 2003/105223 A3



**Published:**

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

**(88) Date of publication of the international search report:**  
16 September 2004

# INTERNATIONAL SEARCH REPORT

International Application No

PCT/IB 03/02094

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L23/31 H01L23/495

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 794 572 A (MATSUSHITA ELECTRONICS CORP) 10 September 1997 (1997-09-10) abstract; figures 1,2,7,8,14,17 column 2, line 53 - column 6, line 11 column 13, line 1 - line 44 claims 1,16	1-5
X	US 6 201 292 B1 (HITOMI YOICHI ET AL) 13 March 2001 (2001-03-13) abstract; figures 4,14,18 column 1, line 40 - column 3, line 41 claim 1	1-5
X	US 2002/063257 A1 (WANG BILY) 30 May 2002 (2002-05-30) abstract; figures 2,4,5,8 page 1, paragraph 24 claim 1	1
A		2-5
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Date of the actual completion of the international search

22 July 2004

Date of mailing of the international search report

02/08/2004

Name and mailing address of the ISA

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# INTERNATIONAL SEARCH REPORT

International Application No

PCT/IB 03/02094

## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 02, 26 February 1999 (1999-02-26) -& JP 10 313082 A (SANYO ELECTRIC CO LTD), 24 November 1998 (1998-11-24)	1
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International Application No

PCT/IB 03/02094

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